REMARKS

Paragraph 2 of the last office action rejects claims 1-13 on the grounds that all of the claims are "obvious" under 35USC103 based on the teachings of US patents 5,864,176 (Babcock) and 5,930,893 (Eaton). In those claims 1-13, claim 1 is the only independent claim and claims 2-13 depend on claim 1. Thus, if claim 1 contains limitations which are not obvious, then all of the claims 1-13 should be in a condition for allowance.

To support the rejection, paragraph 2 of the office action says "Babcock discloses a method and mechanical assembly for testing chips comprising all of the applicant's claimed and disclosed limitations, except for . . . subjecting the layer 102 . . . between the heatsink and electric heater to a crack-healing temperature cycle . . ." (underlining added). However, this quoted statement is not correct. Babcock also does not disclose that any stress cracks will even be induced in the layer 102 when the heatsink and electric heater are subjected to multiple temperature changes in a chip tester.

Babcock shows the layer 102 in Fig. 18, and Babcock describes the layer 102 at lines 21-25 of column 13. No cracks are shown in the layer 102 in Fig. 18, and no cracks are described as occurring in the layer 102 at lines 21-25 of column 13. Thus, there is no teaching in Babcock of the problem that cracks will occur in the layer 102 due to multiple temperature changes. By comparison, claim 1 of the present case expressly recites a "testing" step which "puts said heat-exchanger through multiple temperature changes where said layer stays in a solid state and where stress cracks are induced in said layer".

With regard to Eaton, paragraph 2 of the office action says that the thermally conductive layer in Eaton "under goes a crack-healing temperature cycle in which the layer is at least partially melted and re-solidified" (underlining added). But here again, this quoted statement is not correct. In Eaton, there are no cracks in the thermally conductive layer which is melted. Instead in Eaton, there only are air gaps between the uneven surface of the thermally conductive layer which is melted and the uneven surface of another adjacent component.

Fig. 2 of Eaton shows a gasket 300 which has top and bottom surfaces that are coated with thermally conductive layers. The top layer lies adjacent to the uneven surface 210 of a semiconductor, and the bottom layer lies adjacent to the uneven surface 110 of a heatsink. Since the surfaces 210 and 110 are uneven, air gaps occur between those surfaces and the thermally conductive layer on the gasket 300. See the description of Fig. 2 at lines 59-63 in column 3.

To eliminate the air gaps at the uneven surfaces 210 and 110, the thermally conductive layers on the gasket 300 are melted and re-solidified. This is a one-time operation that occurs only when the semiconductor 200 is initially operated. See Eaton at line 64 of column 2 to line 20 of column 3.

Thus, Eaton completely overlooks the fact that stress cracks can occur in his thermal conductive layers between the semiconductor surface 210 and the heatsink surface 110, if those surfaces are subjected to multiple temperature changes. These stress cracks will occur after the air gaps at the uneven surfaces 210 and 110 have been eliminated. The occurrence of such stress cracks is taught

only by the present application, and their occurrence is expressly recited by the "testing" step in claim 1. Further, the removal of such stress cracks is taught only by the present application, and that removal is expressly recited by the "subjecting" step in claim 1.

Based on all of the differences which have been pointed out above between claim 1 and the two cited patents (5,864,176 and 5,930,893), it is respectfully submitted that the invention as recited in claim 1 is not obvious. Thus, claim 1 as well as its accompanying dependent claims 2-13 should now be in a condition for allowance.

Accordingly, an early Notice of Allowance is requested.

Respectfully submitted,

By [signature]
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Patti S. Preddy [signature]